Low-Power COS/MOS* Memory 16-Bit NDRO Type

CD4005
CD4005D

Monolithic Silicon

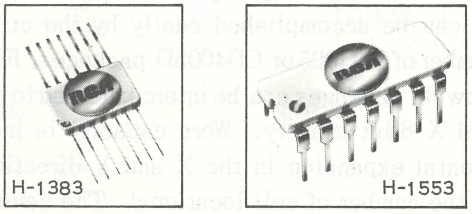
Complementary MOS "N" and "P" Channel 16-Bit NDRO Memory

RCA CD4005 and CD4005D are 16 word, 1 bit deep, non-destructive readout (NDRO) memories consisting of 16 flip-flop storage cells that are arranged in a X-Y matrix for easy access. Addressing and sensing can be accomplished with MOS or bipolar transistor circuits.

The CD4005 is hermetically sealed in a 14-lead ceramic and metal flat-pack. The CD4005D is electrically identical to the CD4005 and is hermetically sealed in a 14-lead, dual-in-line, ceramic and metal package. Terminal configuration and numbering is identical for both types.

Each storage cell contains a flip-flop, which consists of two cross-coupled complementary-symmetry MOS inverter stages, and two transmission gates**. Each transmission gate consists of two n-channel MOS transistors which are connected to perform the gating to and from each cell.

Memory systems utilizing the CD4005 or CD4005D have extremely low power dissipation at high operating speeds. Other advantages are direct logic-level addressing and writing, and a choice of either logic-level or current-sensing readout.



CD4005 CD4005D

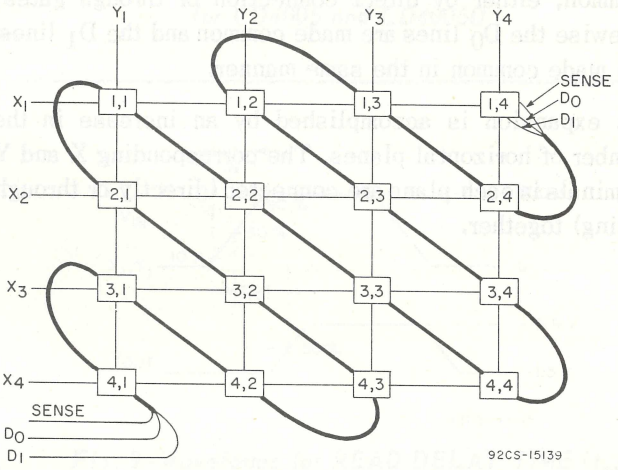


Fig. 1 - Cell-Arrangement Diagram

FEATURES:

- 100 nW quiescent power dissipation
- 15 ns readout delay time (with bipolar amplifier current sensing)
- operation from single positive or negative 10-volt (typical) supply
- Full military temperature range - - -55° C to 125° C
- Diode protection at all MOS gate input points

*Complementary-symmetry metal-oxide-semiconductor
**Bidirectional gate

MODE OF OPERATION

Addressing of a particular cell is accomplished by the simultaneous application of high voltage levels on the X-Y coordinates of that cell. A "1" is written into an addressed cell by the application of a low voltage level on the D_1 line and a high voltage level on the D_0 line; conversely, a "0" is written into the addressed cell by forcing the D_0 line "low" and the D_1 line "high". Non destructive readout (NDRO), or sensing, at the $\overline{Q}$-sense return line of an addressed cell is accomplished by providing sense current by means of an externally forced high-level voltage on the D_1 line. The D_0 line is also maintained at a high-voltage level during readout.

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Sensing can also be accomplished by external logic-level monitoring of the D_0 and D_1 lines. In this mode of sensing logic circuitry must be provided that will inhibit the writing operation during readout, and the sense line must be connected to V_{SS}.

EXPANSION of CD4005 or CD4005D

Expansion of this memory beyond the 16 word one-bit capacity can be accomplished easily by the utilization of any number of CD4005 or CD4005D packages. Figure 2 shows how 32 packages can be interconnected to produce a 64-word X 8-bit memory. Word capacity is increased by horizontal expansion in the X and Y directions (increasing the number of cell locations). The sense lines in each plane (each plane represents one bit) are made common, either by direct connection or through gates; likewise the D_0 lines are made common and the D_1 lines are made common in the same manner.

Bit expansion is accomplished by an increase in the number of horizontal planes. The corresponding X and Y terminals in each plane are connected (directly or through gating) together.

EXAMPLE

To write the binary word 10111011
(least-significant-bit is bit 1)
into word locations 3, 4:

1) X_3 and Y_4 inputs are set to a high level (H)

2)

Bit #	D_0	D_1
1	H	L
2	H	L
3	L	H
4	H	L
5	H	L
6	H	L
7	L	H
8	H	L

To read this same word out of word location 3, 4:

1) X_3 and Y_4 are again set to a high level

2) Current from an external source is supplied on the D_1 line for each bit (D_1 is set to a high level)

3) All D_0 lines are maintained at a high voltage level

All sense leads associated with cells in which a "1" was stored will carry approximately 500 microamperes; those cells containing a "0" will pass virtually zero current through their respective D_1 leads.

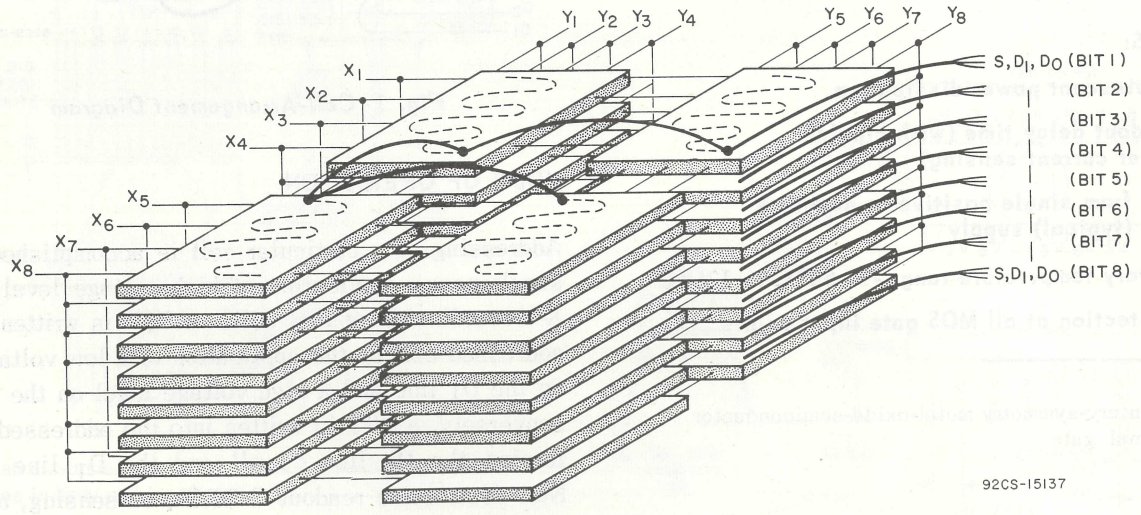


Fig. 2 - 64-Word X 8-Bit Memory Using 32 Packages

ABSOLUTE-MAXIMUM LIMITS:

STORAGE-TEMPERATURE RANGE . . . . . $-65^{\circ}C$ to $+150^{\circ}C$
OPERATING-TEMPERATURE RANGE . . . . $-55^{\circ}C$ to $+125^{\circ}C$
DC SUPPLY VOLTAGE ($V_{DD} - V_{SS}$) . . . . . 15 V
DC CURRENT DRAIN . . . . . 10 mA
ALL INPUTS . . . . . $V_{SS} \leq V_{IN} \leq V_{DD}$

STATIC ELECTRICAL CHARACTERISTICS,
at $T_A = 25^{\circ}C$, $V_{DD} = +10$ V, $V_{SS} = 0$ V

CHARACTERISTICS	SYMBOLS	WHERE MEASURED	SPECIAL TEST CONDITIONS	LIMITS CD4005 & CD4005D			UNITS
				MIN.	TYP.	MAX.	
"0" DC Sense Current	I_S "0"	*See Fig. 6.*	$X_i = Y_j = 10$ V $D_0 = D_1 = 10$ V	–	10	20	μA
"1" DC Sense Current	I_S "1"	*See Fig. 6*	$X_i = Y_j = 10$ V $D_0 = D_1 = 10$ V	500	1000	–	μA
DC Input Current	I_X, I_Y	X_i, Y_j	$V_{IN} = 10$ V $V_{IN} = 0$ V	– –	1 1	– –	nA
Data Input Current	I_{D0}, I_{D1}		$D_0 = D_1 = 10$ V $X_i = Y_j = 10$ V	500	1000	–	μA
			D_0 or $D_1 = 0$ V $X_i = Y_j = 10$ V	–	–1* PEAK	–	mA
Quiescent Device Dissipation	P_T	*See Fig. 7*	All X, Y Inputs and Sense = GND $D_0 = D_1 = 10$ V	–	100	–	nW
Input Capacitance	C_{IN}	X_i, Y_j	$X_i = Y_j = 0$	–	10	15	pF
Output Capacitance	C_{OUT}	D_0, D_1	$D_0 = D_1 = 10$ V	–	20	25	
Sense Line Capacitance	C_{SENSE}	TERM. No.9		–	20	25	

*Pulsed: Pulse Width = 50 ns

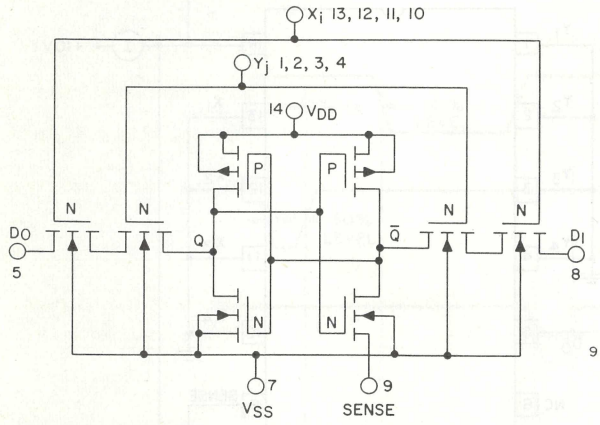
DYNAMIC ELECTRICAL CHARACTERISTICS,
at $T_A = 25^{\circ}C$, $V_{DD} = +10$ V, $V_{SS} = 0$ V, $C_{OUT} = 30$ pF

CHARACTERISTICS	SYMBOLS	TEST SETUPS	LIMITS			UNITS
		FIGS.	MIN.	TYP.	MAX.	
Sense "1" Read Delay Time	t_{rd} "1"	8, 9	–	15	25	ns
Write Pulse Duration	t_w	8, 11	–	50	75	ns

OPERATING CONSIDERATIONS

The leads of these devices are usually soldered to external circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the device against high electric fields. Although a certain degree of protection against such fields is provided by built-in circuitry, it is recommended that this device not be inserted in conventional plastic "snow" or plastic trays of the types frequently used for the storage and transportation of small semiconductor devices.

These units should not be connected into, or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the device. All unused input leads should be connected to the most negative circuit potential. It is recommended that low impedance pulse generators or power supplies connected to the inputs of this device be removed before the power supply is turned off. This precaution will prevent the signal on the gate from exceeding the power supply voltage and thus prevent possible damage to the protective circuitry.



NOTE: V_{DD}, V_{SS}, D_0, D_1 AND SENSE LINES ARE COMMON TO ALL 16 CELLS.

X_i= X_1 OR X_2 OR X_3 OR X_4

Y_i= Y_1 OR Y_2 OR Y_3 OR Y_4

X AND Y LINES ARE COMMON TO FOUR CELLS EACH AND ARE CONNECTED IN MATRIX FORMAT.

Fig. 3 - Schematic Diagram – One of 16 Memory Cells

TRUTH TABLE (EACH CELL)

WRITING VIA D_0 and D_1 LINES

X	Y	D_0	D_1	CELL STATUS	SENSE CURRENT (mA)
0	0	X	X	NC	0
1	0	X	X	NC	0
0	1	X	X	NC	0
1	1	0	0	U	0
1	1	1	0	1	0
1	1	0	1	0	0
CURRENT SENSING AT "SENSE" LEAD					
1	1	1	1	1	0.5
1	1	1	1	0	0
LOGIC-LEVEL SENSING ON D_0 & D_1 LEADS					
1	1	Q	$\bar{Q}$	NC	"sense" line shorted to V_{SS}

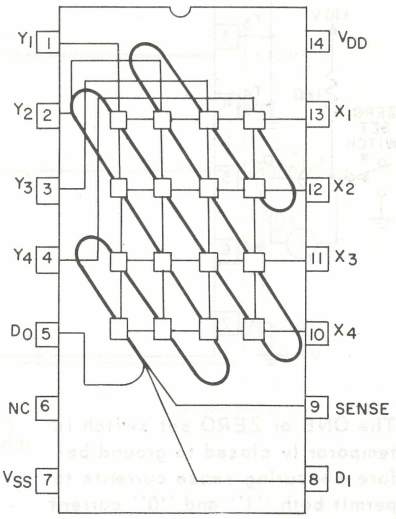
POSITIVE LOGIC

Levels { "0" = V_{SS} ; "1" = V_{DD}

X = DON'T CARE

NC = NO CHANGE

U = UNDETERMINABLE



NOTE: ALL UNUSED INPUTS MUST BE CONNECTED TO THE MOST NEGATIVE CIRCUIT VOLTAGE (V_{SS}).

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Fig. 4 - Functional Diagram for CD4005 and CD4005D

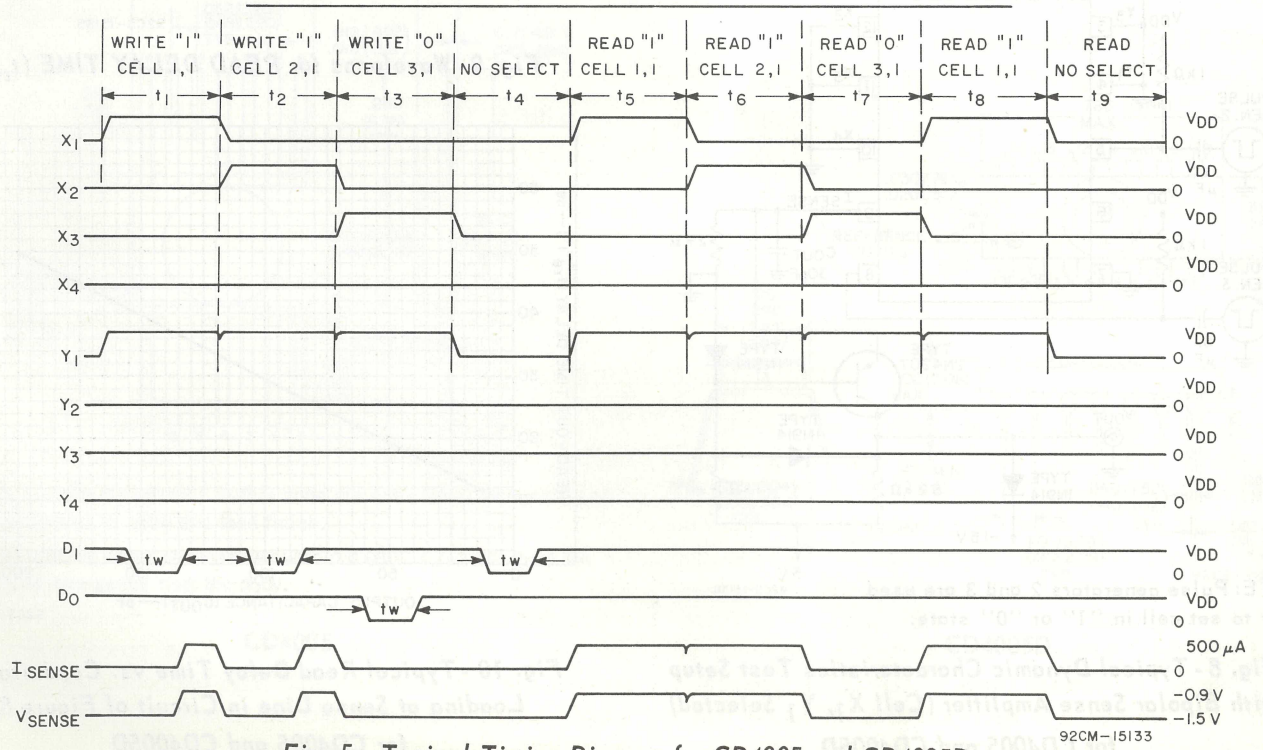
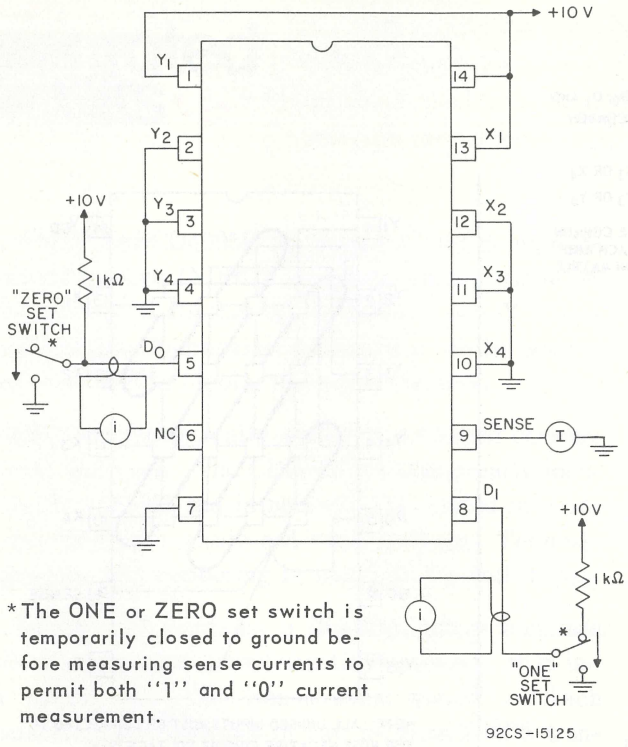


Fig. 5 - Typical Timing Diagram for CD4005 and CD4005D



*The ONE or ZERO set switch is temporarily closed to ground before measuring sense currents to permit both "1" and "0" current measurement.

Fig. 6 - Test Circuit for Measurement of Sense Current from Cell X_1, Y_1 for CD4005 and CD4005D (Typical of results obtained from the other 15 cells)

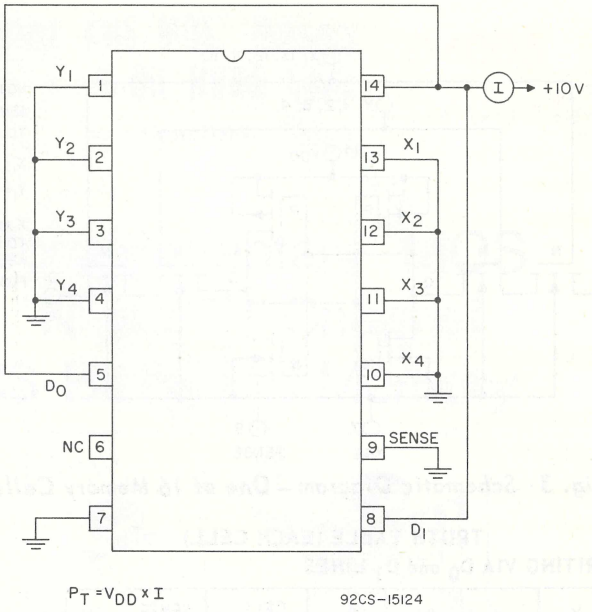


Fig. 7 - Quiescent Device Dissipation Test Setup for CD4005 and CD4005D

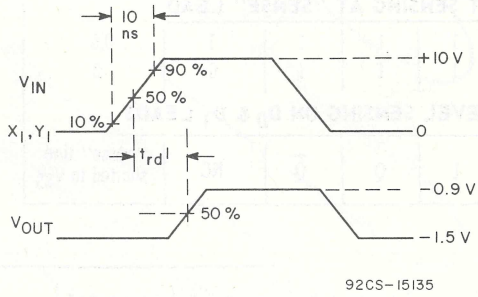
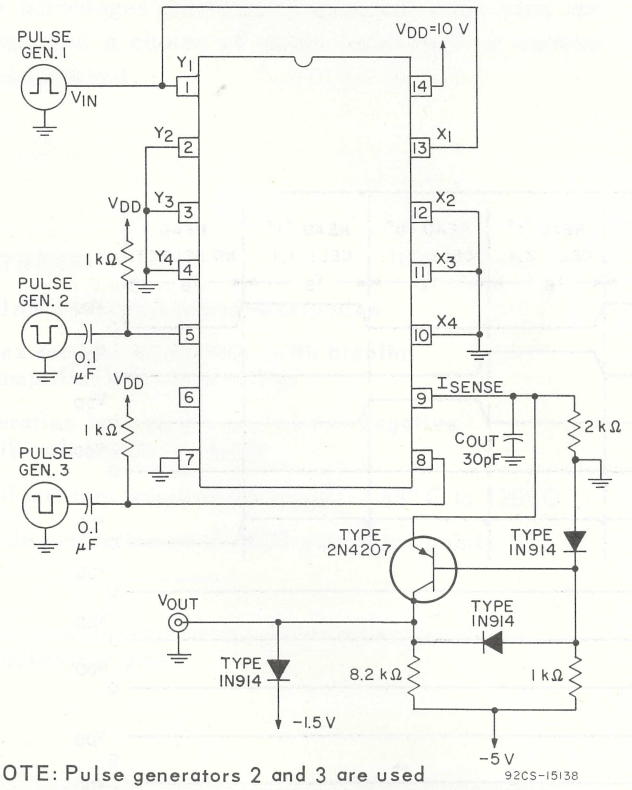


Fig. 9 - Waveforms for READ DELAY TIME (t_{rd})



NOTE: Pulse generators 2 and 3 are used only to set cell in "1" or "0" state.

Fig. 8 - Typical Dynamic Characteristics Test Setup with Bipolar Sense Amplifier (Cell X_1, Y_1 Selected) for CD4005 and CD4005D

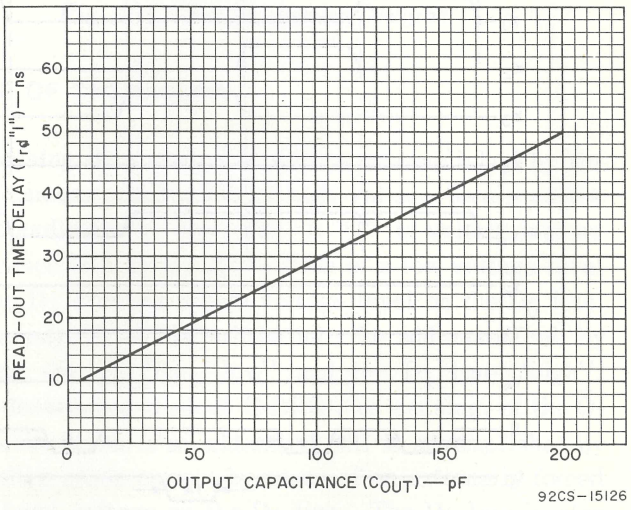


Fig. 10 - Typical Read Delay Time vs. Capacitance Loading at Sense Line in Circuit of Figure 8 for CD4005 and CD4005D

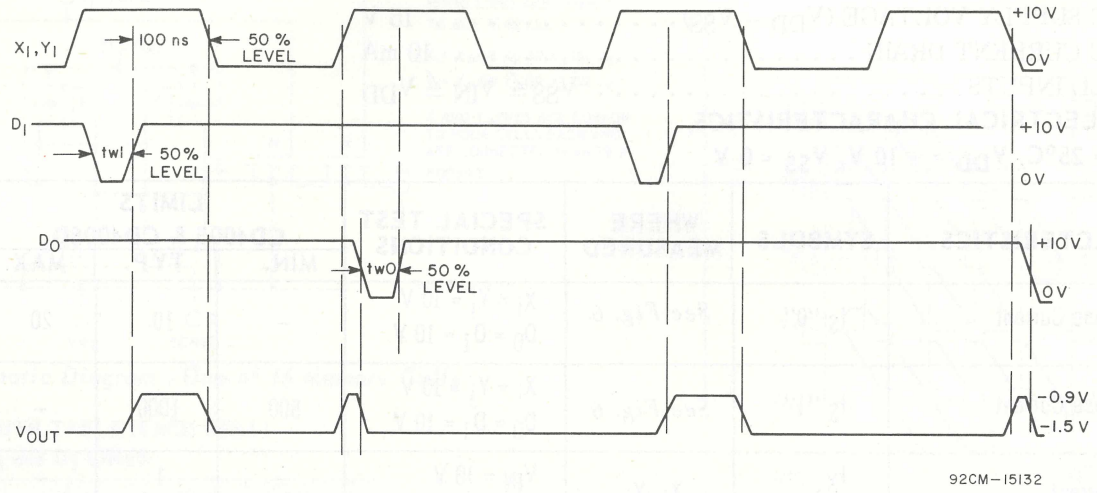
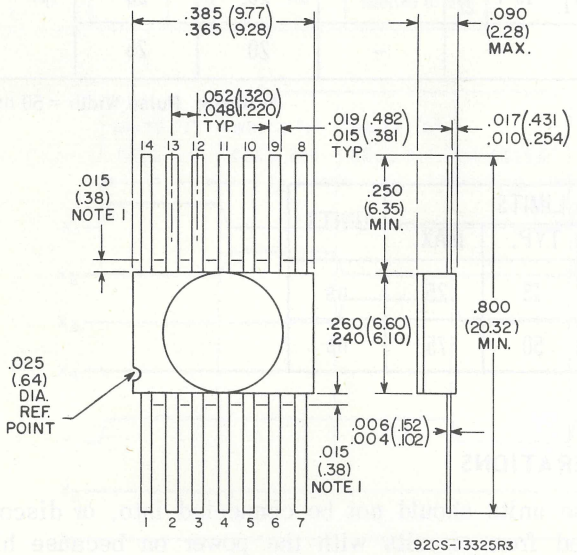


Fig. 11 - Waveforms for Determining Minimum WRITE TIME Pulse Duration (t_W)

DIMENSIONAL OUTLINES

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.

14-LEAD CERAMIC-AND-METAL FLAT PACK



Note 1: Lead dimensions in this zone are not controlled because of irregularities in body and lead finish.

Lead spacing shall be measured within 0.030" (.762 mm) from the point of emergence from the body.

CD4005

14-LEAD CERAMIC-AND-METAL DUAL-IN-LINE PACKAGE

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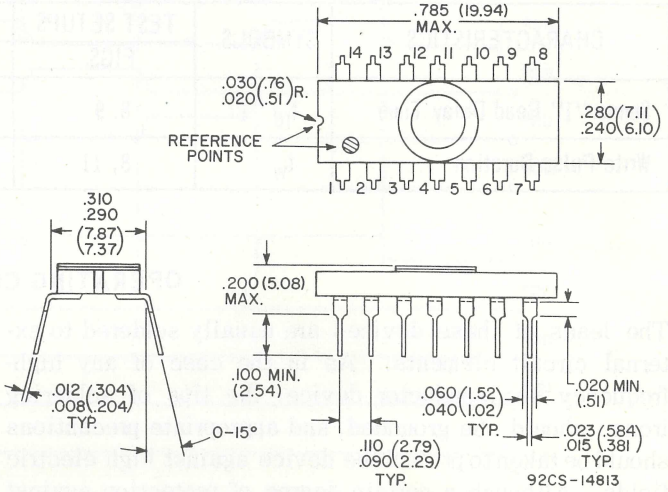

CD4005D